UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,997	10/30/2003	Tsutomu Hatakeyama	244741US2	5655

22850 7590 10/27/2005

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
IWASHKO, LEV	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 10/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,997	HATAKEYAMA, TSUTOMU	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/30/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because Figure 3 is incorrect. There is some illegible and incomprehensible script below the drawing, which makes it difficult to understand what is being referenced.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112, 2nd Paragraph

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4, 11, and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The following claims show insufficient antecedent basis:

Claims 4 (line 10), 11 (line 10), and 17 (line 7) all reference "a unit of one way". It is unclear what a "unit of one way" is, as it was not clearly defined in the specification. It is the inventor's responsibility to thoroughly define every term that is used or referenced in the claims.

Claim Rejections - 35 USC § 102

4. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3-8, 10-14, and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by White et al. (US Patent 5,696,937)

Claim 1. A cache memory, comprising:

- a data storage capable of storing data which requires consistency of data with a main memory; *(Column 1, lines 40-43 – State that there should always exist cache coherency between two stored items of information in a main memory and a cache memory. In other words, there should be consistency of data)*
- and a storage controller which controls to store data which does not require consistency of data with said main memory in an *(Column 12, lines 15-20 – Declare an invalidation queue address storage unit which includes the logic to control queue operation)*

- arbitrary data region in said data storage. *(Column 1, lines 28-29 – States that a cache stores data, so is therefore a data region. Any data region is an arbitrary data region)*

Claim 3. The cache memory according to claim 1, further comprising:

- a region designating unit which specifies addresses of said data region for storing data which does not require consistency of data with said main memory; *(Column 6, lines 5-6 – State that the "selection of which address is to be used is made by the External State Machine", (a.k.a. region designating unit)*
- and an address coincidence determination unit which determines whether or not the designated address coincides with the addresses designated by said region designated unit. *(Column 3, lines 34-38 – State that there is an invalidation queue (a.k.a. address coincidence determination unit) that acts in conjunction with the external state machine to provide invalidation of addresses)*

Claim 4. The cache memory according to claim 3, further comprising a tag unit which stores addresses of data stored in said data storage, *(Column 5, lines 26-27 – State that there is a tag field with an index)*

- wherein said data storage and said tag unit are composed of a plurality of ways including a plurality of indexes, respectively; *(Column 5, line 47 – States that there are indices)*
- and said region designated unit specifies whether or not data which does not require consistency of data with said main memory is stored in the corresponding data region unit is a unit of one way. *(Column 6, lines 5-6 – State that the "selection of which address to be used is made by the External State Machine". Assuming that "a unit of one way" means a unit that has a particular design, the above statement denotes that the External State Machine selects which address to use, so it could be one that either does or does not require consistency of data)*

Claim 5. The cache memory according to claim 4, further comprising:

- a refill information storage which stores history information of refill in said data storage; *(Column 3, lines 1-4 – State that the refill cycle is managed by a state machine system (a.k.a. refill information storage)*
- and a refill object selector which selects ways to be refilled based on the history information stored in said refill information storage and addresses designated by said region designating unit. *(Column 17, lines 9-11- "The bus interface unit provides a data channel to fill the cache data RAM". This means that there is a selector that selects information to refill)*

Claim 6. The cache memory according to claim 5, wherein region designated unit includes:

- an address setting unit provided for each way, which sets addresses of data region for storing data which does not require consistency of data with said main memory; *(Column 6, lines 5-6 – State that the "selection of which address is to be used is made by the External State Machine", (a.k.a. address setting unit)*
- and a setting information storage provided for each way, which stores flag information indicative of whether or not a prescribed address is set to said address setting unit, *(Column 16, lines 44-45 - State that the invalidation queue (a.k.a setting information storage) checks for correct parity)*
- wherein said refill object selector selects the way to be refilled based on the refill history information and the flag information. *(Column 17, lines 9-11- "The bus interface unit provides a data channel to fill the cache data RAM". This means that there is a selector that selects information to refill)*

Claim 7. The cache memory according to claim 1,

- wherein a look-aside type connection method in which said main memory and said cache memory are connected to a common system

bus, *(Column 4, lines 26-29 – State that there is a CPU connected to a cache memory via a bus)*

- and a write-through writing method in which data is written to said main memory and said cache memory at the same time are adopted. *(Column 1, lines 59-65)*

Claim 8. A processor which adopts a look-aside type connection method in which a main memory and a cache memory are connected to a common system bus, and a write-through writing method in which data is written to said main memory and said cache memory at the same time, wherein said cache memory includes:

- a data storage capable of storing data which requires consistency of data with said main memory; *(Column 1, lines 40-43 – State that there should always exist cache coherency between two stored items of information in a main memory and a cache memory. In other words, there should be consistency of data)*
- and a storage controller which controls to store data which does not require consistency of data with said main memory, *(Column 12, lines 15-20 – Declare an invalidation queue address storage unit which includes the logic to control queue operation)*
- in an arbitrary data region in said data storage. *(Column 1, lines 28-29 – States that a cache stores data, so is therefore a data region. Any data region is an arbitrary data region)*

Claim 10. The processor according to claim 8, further comprising:

- a region designated unit which specifies addresses of said data region to store data which does not require consistency of data with said main memory; *(Column 6, lines 5-6 – State that the "selection of which address is to be used is made by the External State Machine", (a.k.a. region designating unit)*
- and an address coincidence determination unit which determines whether or not the designated address coincides with the address

designated by said region designated unit. *(Column 3, lines 34-38 – State that there is an invalidation queue (a.k.a. address coincidence determination unit) that acts in conjunction with the external state machine to provide invalidation of addresses)*

Claim 11. The processor according to claim 10,

- further comprising a tag unit which stores addresses of data stored in said data storage, wherein said data storage and said tag unit are composed of a plurality of ways including a plurality of indexes, respectively; *(Column 5, line 47 – States that there are indices)*
- and said region designated unit specifies whether or not data which does not require consistency of data with said main memory is stored in the corresponding data region unit is a unit of one way. *(Column 6, lines 5-6 – State that the "selection of which address to be used is made by the External State Machine". Assuming that "a unit of one way" means a unit that has a particular design, the above statement denotes that the External State Machine selects which address to use, so it could be one that either does or does not require consistency of data)*

Claim 12. The processor according to claim 11, further comprising:

- a refill information storage which stores history information of refill in said data storage; *(Column 3, lines 1-4 – State that the refill cycle is managed by a state machine system (a.k.a. refill information storage)*
- and a refill object selector which selects ways to be refilled based on the history information stored in said refill information storage and addresses designated by said region designating unit. *(Column 17, lines 9-11- "The bus interface unit provides a data channel to fill the cache data RAM". This means that there is a selector that selects information to refill)*

Claim 13. The processor according to claim 12, wherein region designated unit includes:

- an address setting unit provided for each way, which sets addresses of data region for storing data which does not require consistency of data with said main memory; *(Column 6, lines 5-6 – State that the "selection of which address is to be used is made by the External State Machine", (a.k.a. address setting unit)*
- and a setting information storage provided for each way, which stores flag information indicative of whether or not a prescribed address is set to said address setting unit, *(Column 16, lines 44-45 - State that the invalidation queue (a.k.a setting information storage) checks for correct parity)*
- wherein said refill object selector selects the way to be refilled based on the refill history information and the flag information. *(Column 17, lines 9-11- "The bus interface unit provides a data channel to fill the cache data RAM". This means that there is a selector that selects information to refill)*

Claim 14. A cache control method

- which adopts a look-aside type connection method in which a main memory and a cache memory are connected to a common system bus, *(Column 2, lines 43-55 – State that the main memory and cache both have data in common addresses, which could not occur without the same bus)*
- and a write-through writing method in which data is written into said main memory and said cache memory at the same time, comprising controlling to store data which does not require consistency of data with said main memory *(Column 1, lines 60-65 – Describes the "Write through method")*
- in an arbitrary data region in a data storage to store data which does not require consistency of data said main memory. *(Column 1, lines 28-29 – States that a cache stores data, so is therefore a data region. Any data region is an arbitrary data region)*

Claim 16. The cache control method according to claim 14, further comprising:

- designating in advance addresses of said data region to store data which does not require consistency of data with said main memory; *(Column 6, lines 5-6 – State that the "selection of which address is to be used is made by the External State Machine", (a.k.a. region designating unit)*
- and determining whether or not required address coincides with the designated address. *(Column 3, lines 34-38 – State that there is an invalidation queue (a.k.a. address coincidence determination unit) that acts in conjunction with the external state machine to provide invalidation of addresses)*

Claim 17. The cache control method according to claim 16,

- wherein said data storage and a tag unit which stores addresses of data stored in said data storage are composed of a plurality of ways including a plurality of indexes; *(Column 5, line 47 – States that there are indices)*
- and it is designated whether or not data which does not require consistency of data with said main memory is stored in the corresponding data region unit in unit of one way. *(Column 6, lines 5-6 – State that the "selection of which address to be used is made by the External State Machine". Assuming that "a unit of one way" means a unit that has a particular design, the above statement denotes that the External State Machine selects which address to use, so it could be one that either does or does not require consistency of data)*

Claim 18. The cache control method according to claim 17, further comprising:

- storing history information of refill in said data storage; *(Column 17, lines 9-11- "The bus interface unit provides a data channel to fill the cache data RAM". This means that there is data which is stored)*
- and selecting the way to be refilled based on the stored history information and the address designated by said region designated unit.

(Column 17, lines 9-11- "The bus interface unit provides a data channel to fill the cache data RAM". This means that there is a selector that selects information to refill in a particular address)

Claim 19. The cache control method according to claim 18, comprising:

- setting addresses of a data region to store data which does not require consistency of data with said main memory for each way; *(Column 6, lines 5-6 – State that the "selection of which address is to be used is made by the External State Machine", (a.k.a. address setting unit)*
- storing the flag information indicative of whether or not addresses are set for each way; *(Column 16, lines 44-45 - State that the invalidation queue (a.k.a setting information storage) checks for correct parity)*
- and selecting the way to be refilled based on said refill history information and said flag information. *(Column 17, lines 9-11- "The bus interface unit provides a data channel to fill the cache data RAM". This means that there is a selector that selects information to refill)*

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 2 is rejected under 35 U.S.C.103(a) as being unpatentable over White as applied to claim 1 above.

White teaches the limitations of claim 1 for the reasons above.

White's invention differs from the claimed invention in that there is no specific reference to allowing a programmer to be the one to designate a data region.

White fails to teach claim 2, which states "The cache memory according to claim 1, wherein said arbitrary data region is a data region designated by a programmer." However, stating that a programmer can designate the data region does not change the purpose or functionality of the data region itself. Making something able to be designated by a programmer is like making it adjustable. Therefore, it would have been obvious to one of ordinary skill in the art to declare the data region of White to be allowably designated by a programmer in order to allow for the programmer to declare a data region of any feasible size for the purpose of convenience and personal preference.

For further information, reference Stevens (212 F.2d 197, 101 USPQ 284 (CCPA 1954)), which states the following: "The court held that adjustability, where needed, is not a patentable advance".

8. Claim 9 is rejected under 35 U.S.C.103(a) as being unpatentable over White as applied to claim 8 above.

White teaches the limitations of claim 8 for the reasons above.

White's invention differs from the claimed invention in that there is no specific reference to allowing a programmer to be the one to designate a data region.

White fails to teach claim 9, which states "The processor according to claim 8, wherein said arbitrary data region is a data region designated by a programmer." However, stating that a programmer can designate the data region does not change the purpose or functionality of the data region itself. Making something able to be designated by a programmer is like making it adjustable. Therefore, it would have been obvious to one of ordinary skill in the art to declare the data region of White to be allowably designated by a programmer in order to

allow for the programmer to declare a data region of any feasible size for the purpose of convenience and personal preference.

For further information, reference Stevens (212 F.2d 197, 101 USPQ 284 (CCPA 1954)), which states the following: "The court held that adjustability, where needed, is not a patentable advance".

9. Claim 15 is rejected under 35 U.S.C.103(a) as being unpatentable over White as applied to claim 14 above.

White teaches the limitations of claim 14 for the reasons above.

White's invention differs from the claimed invention in that there is no specific reference to allowing a programmer to be the one to designate a data region.

White fails to teach claim 15, which states "The cache control method according to claim 14, wherein said arbitrary data region is a data region designated by programmer." However, stating that a programmer can designate the data region does not change the purpose or functionality of the data region itself. Making something able to be designated by a programmer is like making it adjustable. Therefore, it would have been obvious to one of ordinary skill in the art to declare the data region of White to be allowably designated by a programmer.

For further information, reference Stevens (212 F.2d 197, 101 USPQ 284 (CCPA 1954)), which states the following: "The court held that adjustability, where needed, is not a patentable advance".

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

MATTHEW D. ANDERSON
PRIMARY EXAMINER